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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/726,042 | 12/01/2003 | Nikhil V. Kelkar | NSC1P284 | 2661 |

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| EXAMINER | |
|---|---|
| NGUYEN, DAO H | |
| ART UNIT | PAPER NUMBER |
| 2818 | |

DATE MAILED: 09/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/726,042 | KELKAR ET AL. | |
| | Examiner | Art Unit | |
| | Dao H. Nguyen | 2818 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *01 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *16-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *0404*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. This Office Action is in response to the communications dated 12/01/2003 through 09/01/2005.

Claims 1-20 are active in this application.

### Acknowledges

2. Receipt is acknowledged of the following items from the Applicant.

Information Disclosure Statement (IDS) filed on 04/05/2004. The references cited on the PTOL 1449 form have been considered.

Applicant is requested to cite any relevant prior art if being aware on form PTO-1449 in accordance with the guidelines set for in M.P.E.P. 609.

### Election/Restriction

3. Application's election with traverse to prosecute the invention of Group I, claims 1-15, drawn to semiconductor devices, filed 09/01/2005 is acknowledged.

The traversal is on the ground(s) that see the election paper. This is not found persuasive because the fields of search for method claims, which is classified in class 438, and device claims, which is classified in class 257, are NOT coextensive and the determinations of patentability of method and device claims are different, that is process

limitations and device limitations are given weight differently in determining the patentablitity of the claimed inventions. Also, the strategies for doing text searching of the device claims and method claims are different. Thus, separate searches are required.

The requirement is still deemed proper and is therefore made **FINAL**.

Claims 16-20 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a non-elected group there being no allowable generic or linking claim.

Applicant has the right to file a divisional application covering the subject matter of the non-elected claims.

4. Applicant is reminded that a complete reply to this Office Action should include cancellation of nonelected claims or other appropriate action (37 CFR 1.144). See MPEP § 821.01. Also, upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a diligently filed petition under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(h).

**Specification**

5. The specification has been checked to the extent necessary to determine the presence of possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

## Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claim(s) 8 is rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent No. 6,258,705 to Chien et al.

Regarding claim 8, Chien discloses an integrated circuit device 100, as shown in figs. 5, comprising:

a plurality of contact pads 113 formed on a first surface of said device 100;

a plurality of under bump metallization stacks 132, wherein one or more of said plurality of under bump metallization stacks 132 each couple with an associated contact pad 113, and wherein each such under bump metallization stack comprises a plurality of metal or alloy layers (copper layer 130a, and Nickel-Vanadium layer 130b), none of which are an aluminum layer, a titanium layer or a chromium layer. See also col. 5, line 22 to col. 6, line 49.

8. Claim(s) 8-11,and 13-15 are rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent No. 6,452,270 to Huang.

Regarding claim 8,Huang discloses an integrated circuit device 310, as shown in fig. 7, comprising:

a plurality of contact pads 320 formed on a first surface of said device 310;

a plurality of under bump metallization stacks 340(c-d), wherein one or more of said plurality of under bump metallization stacks each couple with an associated contact pad 320, and wherein each such under bump metallization stack 340(c-d) comprises a plurality of metal or alloy layers 340(c-d), none of which are an aluminum layer, a titanium layer or a chromium layer. See also col. 3, line 38 to col. 4, line 45. See also the abstract.

Regarding claim 9, Huang discloses the integrated circuit device further comprising:

a resilient layer 340a disposed on said first surface, said resilient layer 340a having a plurality of vias formed therethrough, wherein one or more of said plurality of vias defines a primary axis extending therethrough (a primary axis extending, within the vias, diagonally from the top surface to the bottom surface of the resilient layer 340a) and one or more sidewalls (extending vertically from the top surface to the bottom surface of the resilient layer 340a) that are not substantially parallel to said primary axis. See fig. 7.

Regarding claim 10, Huang discloses the integrated circuit device wherein at least a portion of said plurality of under bump metallization stacks each comprise at least one layer selected from the group consisting of copper (layer 340d) and nickel-vanadium (layer 340c). See col. 1, lines 51-54.

Regarding claim 11, Huang discloses the integrated circuit device wherein at least a portion of said plurality of under bump metallization stacks each comprise a copper layer 340d directly atop and in substantial contact with a nickel-vanadium layer 340c, which is in turn directly atop and in substantial contact with an associated contact pad 320 & 340b (both layers 320 & 340b are formed of copper, and therefore can be considered as a contact pad as a whole).

Regarding claim 13, Huang discloses the integrated circuit device further comprising a passivation layer 330 disposed on said first surface, wherein at least a portion of said at least one passivation layer 330 is located between said first surface and said resilient layer 340a. See fig. 7.

Regarding claim 14, Huang discloses the integrated circuit device wherein said passivation layer 330 comprises a plurality of passivation layer vias formed therethrough, wherein one or more of said plurality of passivation layer vias each define a perimeter that completely encloses the perimeter of a corresponding resilient layer via. See fig. 7.

Regarding claim 15, Huang discloses the integrated circuit device further comprising a plurality of solder bumps 350, wherein one or more of said plurality of solder bumps 350 are each coupled with an associated under bump metallization stack and an associated contact pad. See fig. 7.

**Claim Rejections - 35 U.S.C. § 103**

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claim(s) 1 is rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,258,705 to Chien et al., in view of the following remarks.

Regarding claim 1, Chien discloses a semiconductor device, as shown in figs. 5, comprising:

a die 100 having a plurality of contact pads 113 formed on the active surface of the die 100;

a resilient layer 120 disposed on the active surface of said die, said resilient

layer 120 having a plurality of vias 122 formed therethrough, wherein sidewalls of at least some of said plurality of vias 122 are tapered at an angle relative to the active surface of said die;

a plurality of under bump metallization stacks 132 (fig. 5G), each under bump metallization stack including a nickel-vanadium layer 130b and a copper layer 130a, wherein the nickel-vanadium layer 130b is directly atop and in substantial contact with an associated contact pad 113 and the copper layer 130a is directly atop and in substantial contact with the nickel-vanadium layer 130b, said under bump metallization stack 132 being arranged such that at least some portion of the under bump metallization stack 132 overlies a portion of said resilient layer 120; and

a plurality of solder bumps 150, each solder bump 150 being formed on an associated under bump metallization stack 132. See also col. 5, line 22 to col. 6, line 49.

Chien is silent about a semiconductor wafer having an active surface comprising a plurality of dice formed thereon. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made that forming a plurality of dice on an active surface of a semiconductor wafer is very well known and common in semiconductor technology. Such formation is used to reduce the cost and time for forming the dice (in contract to forming dice singly and separately), and/or to integrate multiple dice in the same package. Therefore, this limitation has no patentable weight.

11. Claim(s) 1-7 and 12 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,452,270 to Huang, in view of the following remarks.

Regarding claim 1, Huang discloses a semiconductor device, as shown in fig. 7, comprising a die (see the abstract, lines 1-3), each die having a plurality of contact pads 320 & 340b (both layers 320 & 340b are formed of copper, and therefore can be considered as a contact pad as a whole) formed on the active surface of the substrate 310;

a resilient layer 330/340a disposed on the active surface of said substrate 310, said resilient layer 330/340a having a plurality of vias formed therethrough, wherein sidewalls of at least some of said plurality of vias are tapered at an angle relative to the active surface of said substrate (the side walls of the vias are tapered at an angle of about 90 degree relative to the active surface of the substrate 310);

a plurality of under bump metallization stacks, each under bump metallization stack including a nickel-vanadium layer 340c and a copper layer 340d, wherein the nickel-vanadium layer 340c is directly atop and in substantial contact with an associated contact pad 320 & 340b and the copper layer 340d is directly atop and in substantial contact with the nickel-vanadium layer 340c, said under bump metallization stack being arranged such that at least some portion of the under bump metallization stack overlies a portion of said resilient layer 330/340a; and

a plurality of solder bumps 350, each solder bump 350 being formed on an associated under bump metallization stack. See also col. 3, line 38 to col. 4, line 45.

Huang is silent about a semiconductor wafer having an active surface comprising a plurality of dice formed thereon. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made that forming a plurality of dice on an active surface of a semiconductor wafer is very well known and common in semiconductor technology. Such formation is used to reduce the cost and time for forming the dice (in contract to forming dice singly and separately), and/or to integrate multiple dice in the same package. Therefore, this limitation has no patentable weight.

Regarding claim 2, Huang discloses the semiconductor device, wherein said at least one resilient layer 330 comprises a polyimide. See col. 3, lines 44-47.

Regarding claims 3-4, and 12, Huang discloses the semiconductor/integrated device comprising all claimed limitations, except for explicitly teach that the plurality of under bump metallization stacks has a total thickness of less than about 15 kilo-angstroms, or less than about 12 kilo-angstroms.

However, It would have been an obvious to one of ordinary skills in the art that the thickness of such stack can be chosen at any suitable value, depending on the desired device, since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955).

Regarding claim 5, Huang disclose the semiconductor device, further comprising:

a passivation layer 330 (in this case, considering the resilient layer to be a single layer 340a) disposed on the active surface of said substrate 310, wherein at least a portion of said passivation layer 330 is located between the active surface of said substrate 310 and said resilient layer 340a. See fig. 7.

Regarding claim 6, Huang discloses the semiconductor device, wherein said passivation layer 330 comprises a compound selected from the group consisting of silicon dioxide and silicon nitride.

Regarding claim 7, Huang discloses the semiconductor device wherein said passivation layer 330 comprises a plurality of passivation layer vias formed therethrough, wherein each of said plurality of passivation layer 330 vias define a perimeter that completely encloses the perimeter of a corresponding resilient layer via. See fig. 7.

**Conclusion**

12. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao H. Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday, 9:00 AM – 6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)272-1787. The fax numbers for all communication(s) is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.

David Nelms
Supervisory Patent Examiner
Technology Center 2800

Dao H. Nguyen
Art Unit 2818
September 25, 2005